YAMAHA LSI

YAC513

2-Channel Floating D/A Converter

■ OUTLINE

YAC513 is floating D/A converter with a 10-bit mantissa block and a 7-step exponent block, which generates analog output of 16-bit dynamic range. It is suitable for the stereo FM sound source LSI such as YMF271 (OPX) or YMF278 (OPL4).

■ FEATURES

- Two-channel floating D/A converter.
- 16-bit dynamic range.
- Internal conversion of MSB first 16-bit digital data to floating point data.
- With buffer operational amplifier, analog output is available easily.
- Built-in analog switches for sample and hold operations.
- One-channel operation is possible.
- Si-gate CMOS process and accurate thin film register.
- 5-9V single power supply.
- 16 pin plastic DIP (YAC513-D) or 16-pin plastic SOP (YAC513-M).

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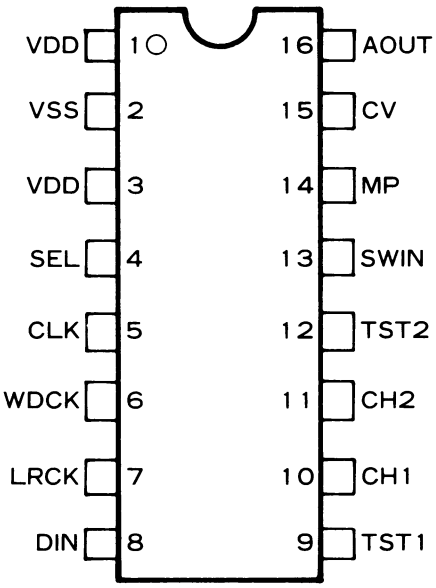
YAC513 CATALOG
CATALOG No. : LSI-4AC5133
1994. 03

■ PIN CONFIGURATION



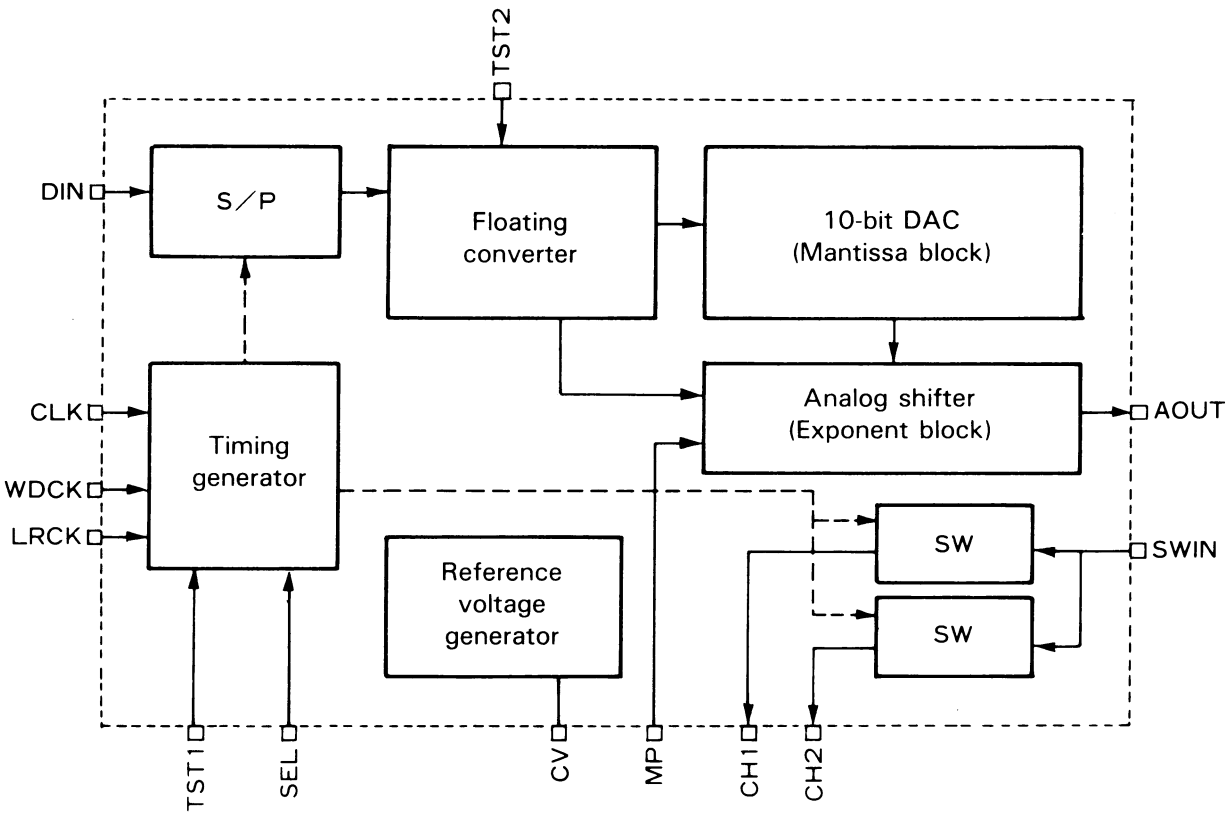
〈 16DIP, 16SOP Top View 〉

■ PIN DESCRIPTION

No.	Pin Name	I/O	Function
1	VDD	—	Power supply (+5 ~ +9V)
2	VSS	—	Ground
3	VDD	—	Power supply (+5 ~ +9V)
4	SEL	I	Selection of operation ('H': 1-channel operation, 'L': 2-channel operation)
5	CLK	I	Digital data input Bit clock
6	WDCK	I	Digital data input Word clock
7	LRCK	I	Digital data input L/R clock
8	DIN	I	Digital data input Serial data (2's complement, MSB first)
9	TST1	I	LSI test terminal (connect to VSS)
10	CH1	OA	Analog switch CH1 output
11	CH2	OA	Analog switch CH2 output
12	TST2	I	LSI test terminal (connect to VSS)
13	SWIN	IA	Analog switch CH1/CH2 common input
14	MP	IA	Analog shifter reference voltage input (bais to 1/2VDD)
15	CV	-A	DAC center voltage terminal (connect to MP terminal via buffer)
16	AOUT	OA	CH1/CH2 analog output (connect to SWIN terminal via buffer)

(Note) A: Analog terminal

■ BLOCK DIAGRAM



■ FUNCTION DESCRIPTION

MSB first serial data synchronized with CLK clock is inputted to DIN terminal and latched on the falling edge of WDCK clock.

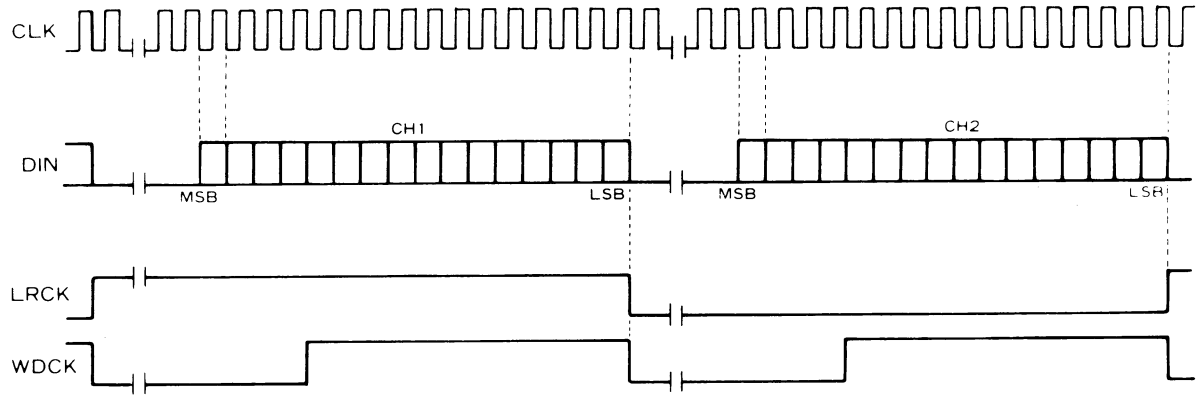
The data is converted to the floating data (10-bit mantissa and 7-step exponent). 10-bit mantissa is sent to the 10-bit DAC and 7-step exponent is sent to the analog shifter. The value determined by this process is outputted to AOUT. The signal outputted from AOUT is inputted to SWIN via buffer OP-AMP. The signal inputted to SWIN is allocated to each channel by analog switch according to LRCK clock and outputted to CH1 or CH2.

Add sample-hold capacitor to CH1 and CH2 to hold analog signal of each terminal period.

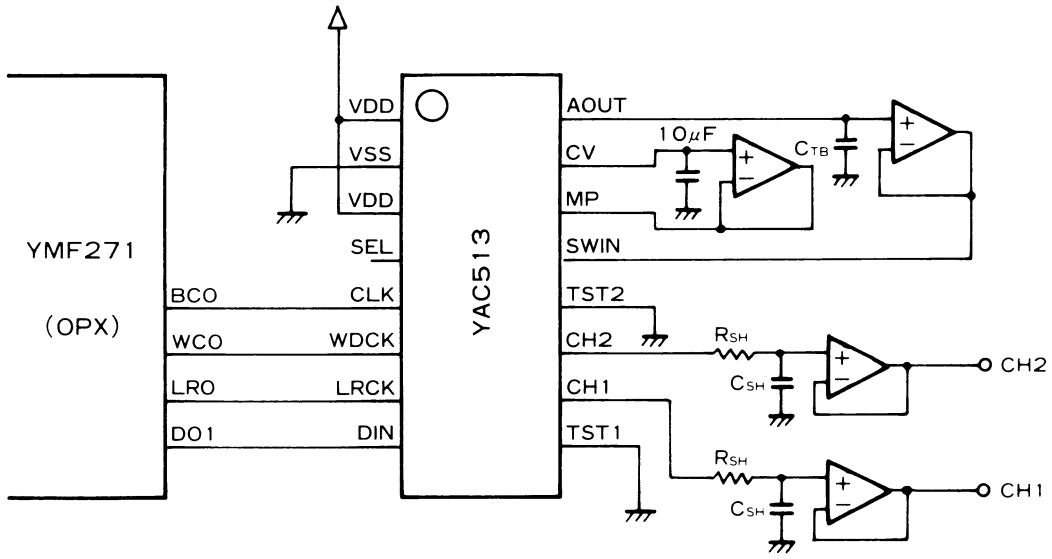
CV outputs 1/2VDD voltage determined by internal resistors. For stabilization, add 10μF capacitor to CV and connect CV to MP via buffer OP-AMP.

When SEL is held to high-level, one-channel operation is selected and analog signals are outputted from CH1 regardless of LRCK clock.

■ INPUT FORMAT



■ SAMPLE CIRCUIT



- recommended conditions
  1) Recommend three-terminal voltage regulator (78 × 05, etc.) for power supply.
  2) Recommend NJM4560, NJM2100 (JRC) for buffer OP-AMP.
     Or recommend following.
     Offset: within 2.0mV
     Through rate: 4V/μs or more
     Output current capability: 20mA or more
  3) Circuit value

	VDD	CTB [pF]	RSH [Ω]	CSH [pF]
16DIP	5 ~ 8V	None	24	1800
	9V	None	39	1800
16SOP	5 ~ 8V	10	360	2200
	9V	10	360	1800

■ ELECTRIC CHARACTERISTICS

1. Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 ~ 15.0	V
Input voltage	V_I	−0.3 ~ V_{DD}+0.5	V
Operating temperature	Top	−25 ~ 70	°C
Storage temperature	Tstg	−50 ~ 125	°C

2. Recommended Operating Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.75	5.00	9.45	V
Operating temperature	Top	−25	25	70	°C

3. DC Characteristics

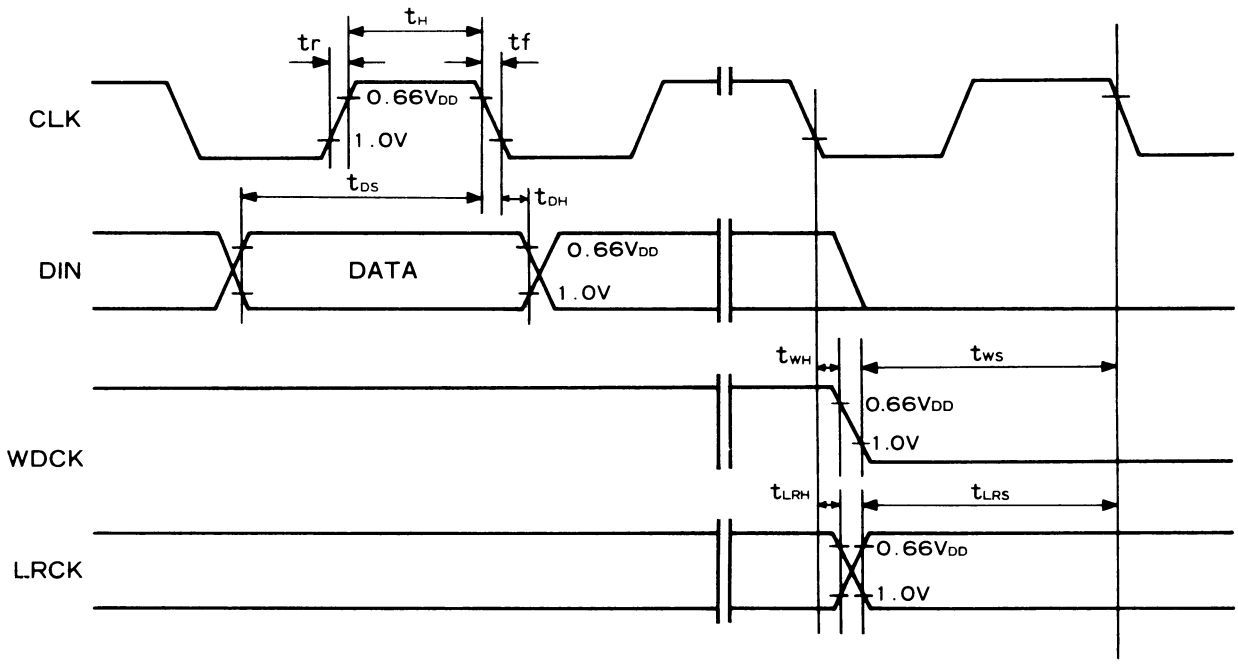
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{DD}	V_{DD}=5.0V			6.0	mA
Input voltage high-level	V_{IH}	*1	0.66V_{DD}			V
Input voltage low-level	V_{IL}	*1			1.0	V
Input leakage current	I_{LK}	*1, V_{DD}=5.0V			1.0	μA
Input capacitance	C_I	*1			5	pF

*1) Applicable to CLK, WDCK, LRCK DIN and SEL terminals.

4. DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK clock frequency	f_C	1.0	8.6	9.0	MHz
high-level time	t_H	55			ns
rise time	t_r			30	ns
fall time	t_f			30	ns
DIN setup time	t_{DS}	60			ns
hold time	t_{DH}	0			ns
WDCK setup time	t_{WS}	40			ns
hold time	t_{WH}	5			ns
LRCK setup time	t_{LRS}	60			ns
hold time	t_{LRH}	0			ns

• DIN timing

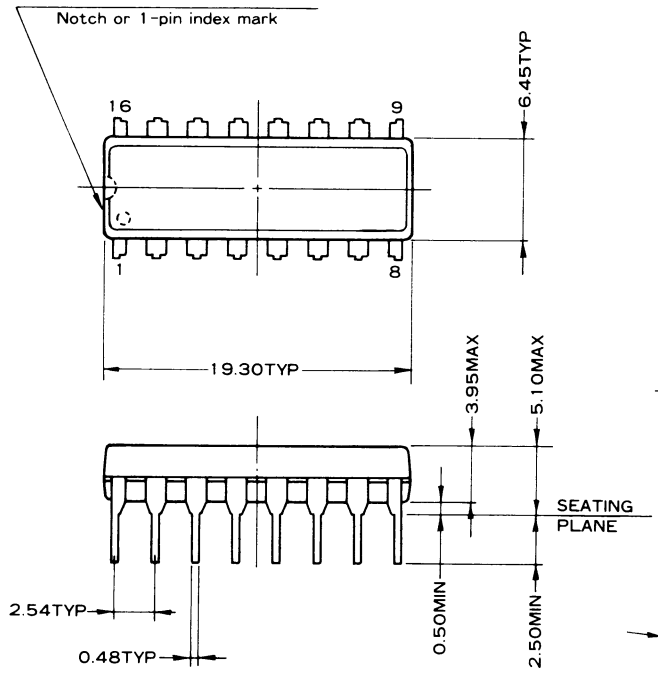


5. Analog Characteristics (Condition: Ta=25°C, VDD=5.0V, measured by sample circuit)

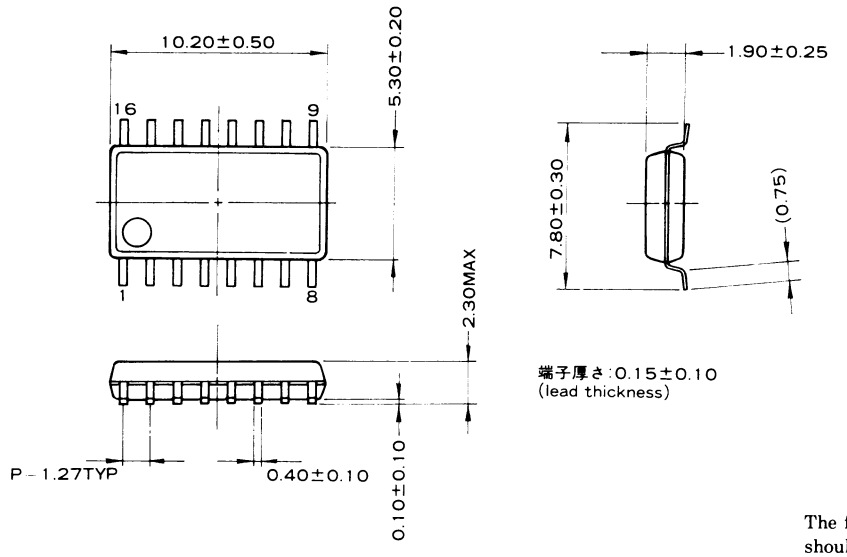
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum output voltage	VO	*1		1/3VDD		V
Total harmonic distortion	THD0	1 KHz, 0dB		0.06	0.15	%
	THD40	1 KHz, −40dB		0.30	0.55	%
Dynamic range	DR			92		dB
Cross talk	CT	1 KHz, 0dB		−73		dB

*1) peaktopeak

■ EXTERNAL DIMENSIONS



Plastic body dimensions do not include burr of resin.
UNIT: mm



The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

The specifications of this product are subject to improvement changes without prior notice.

AGENCY

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